Mid-term Progress Report—Spring 2013

Efficient Resource Utilization in SMT Processors

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Efficient Resource Utilization in SMT Processors

- Goals:
  - Design and implement an algorithm for efficient resource utilization in SMT systems.
  - In this project, we are going to optimize the utilization of write buffer among threads.
- Brief Description
  - In an SMT system, write buffer is shared among threads.
  - Due to its size constraint and potentially long latency from its data, the write buffer becomes the most critical component in an SMT system, which is easily get overwhelming occupied by a thread.

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- Heights of Achievements this semester
  - Proposed an algorithm in commit stage for better allocate resource among threads in an SMT system.
  - Conducted simulations for the algorithm and analyzed the results.

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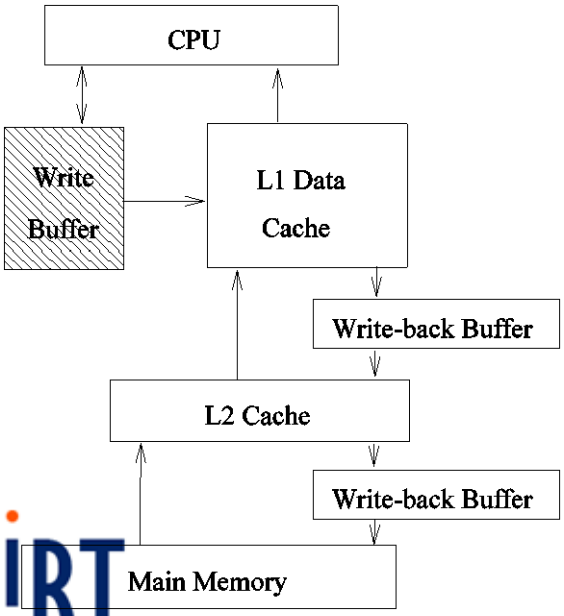
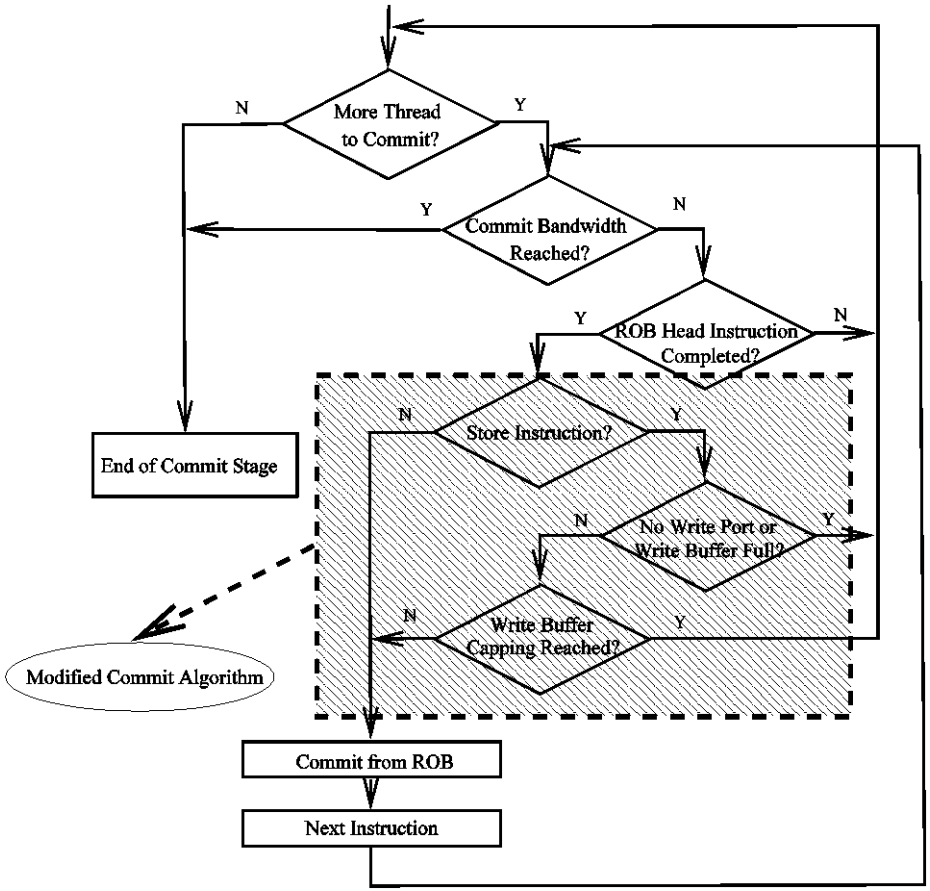
- System configuration
- Flowchart of proposed algorithm





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- Simulation Results
  - Achieved an improvement in IPC of up to 26% and 95% for 4-threaded and 8-threaded workload respectively